COMPOUND SEMICONDUCTOR DEVICE AND ITS MANUFACTURE METHOD

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is based upon and claims the benefit of priority of the prior PCT Application No. PCT/JP2007/053689 filed on Feb. 27, 2007, the entire contents of which are incorporated herein by reference.

FIELD

[0002] The embodiments discussed herein are related to a compound semiconductor device and its manufacture method, and more particularly to a compound semiconductor device having a vertical current path and its manufacture method.

[0003] GaN series (compound semiconductor) indicates $Al_xIn_yGa_{1-x-y}N$ ($0 \leqq x \leqq 1.0$, $0 \leqq y \leqq 1.0$).

BACKGROUND

[0004] Vigorous developments are made for compound semiconductor devices using GaN or GaN series compound semiconductor. GaN has a wide or high band gap of 3.4 eV, and enables a high breakdown voltage operation. Various semiconductor devices can be manufactured using GaN series compound semiconductor.

[0005] GaN has a high breakdown voltage, and is expected to be applied to usage requiring high voltage and high speed operation, such as a high electron mobility transistor (HEMT) for a mobile phone base station. There are various reports on GaN-HEMT formed by growing crystals of GaN/AlGaN on a substrate such as sapphire, SiC, GaN and Si and using a GaN layer as an electron transport or channel layer. A value over 300 V is currently reported as a breakdown voltage in an off-current state. Transistors utilizing the field effect including HEMT and MESFET may collectively called field effect transistors in some cases.

[0006] Metal organic chemical vapor deposition (MOCVD) is mainly used as a crystal growth method. A method called hydride vapor phase epitaxy (H-VPE) is being studied in recent years, which method produces metal chloride by reacting HCl with group III metal and further conducting reaction with ammonia and the like to grow nitride semiconductor.

[0007] If a GaN series field effect transistor of a lateral structure disposing a source, a channel and a drain along a substrate surface layer is used as a power device for vehicles or the like, it is difficult to increase a current density per area so that a chip size becomes large. In order to increase a current density per area, it is preferable to use a vertical structure in which carriers move along a substrate thickness direction.

[0008] JP-A-2003-051508, JP-A-2004-31896, JP-A-2005-203753, and WO2003/071607, which are incorporated herein by reference, propose a vertical structure that a source is disposed on the top surface of a semiconductor substrate, a drain is disposed on the bottom surface, and a gate is disposed on a vertical side wall formed by vertically etching the substrate from the top surface to an intermediate depth. Since a transistor structure is formed along the depth direction of the substrate, it is expected to increase an area utilization efficiency. With this gate electrode structure formed on a vertical side wall formed by vertically etching the semiconductor layer, processes become complicated, and there is a high possibility of many issues such as process precision and yield.

[0009] JP-A-2002-16262, which is incorporated herein by reference, proposes a structure that a source electrode and a gate electrode of interdigital shape are formed on the top surface of a substrate, and a drain electrode is formed on the bottom surface. An n^+-type GaN source region is surrounded by a p-type well and an i-type well, and an n-type GaN channel region is formed under the gate electrode traversing the n-type well and the i-type well. Under the n-type channel region, an n^--type GaN layer, an n^+-type GaN layer and an an n^{++}-type Si substrate are disposed. The electrodes are formed on flat surfaces. In order to electrically separate the source region from the substrate bottom side, a recess is formed by etching, and epitaxial growth on the recess is performed for growing the i-type well, the p-type well and the n^+-type source region. Further a recess is formed by etching, and epitaxial growth on the recess is performed for growing the channel region. It may become necessary to planarize the epitaxial growth surface. It can be considered that manufacture processes are not simple.

[0010] FIG. **5**A schematically illustrates the structure of a vertical type GaN-HEMT reported by University of California, Santa Barbara (Conference Digest of Device Research Conference, 2002, pp. 31-32). An n-type GaN layer **102** is grown on a single crystal sapphire substrate **101**, and a p-type GaN layer **103** serving as a current blocking layer **103** is formed on the n-type GaN layer **102**. The p-type GaN layer **103** is etched to form opening in current flowing region. An n-type GaN layer **105** is grown to fully bury the opening of the current flowing region, and a non-doped GaN active layer **106** serving as an electron transport layer is formed on the p-type GaN layer **103** and the n-type GaN layer **105**. An n-type AlGaN layer **108** serving as an electron supply layer is grown above the non-doped GaN layer **106** via an non-doped AlGaN layer **107** serving as a spacer layer. A deep potential well is formed at the interface of the non-dopes GaN layer contacting the AlGaN layer having a wide band gap, so that two dimensional electron gas 2 DEG is generated. An n-type GaN layer **109** is grown on the n-type AlGaN layer **108**. Isolation is performed by recess etching. A silicon nitride layer **110** is formed on the surface by plasma CVD. The silicon nitride layer on electrode forming areas are removed, and a gate electrode G in Schottky contact and a source electrode S in ohmic contact are formed thereon. The layers down to the n-type GaN layer **102** are etched, and a drain electrode D is formed on the n-type GaN layer **102**.

[0011] FIG. **5**B illustrates the characteristics of the GaN-HEMT thus formed. Drain current Ids does not become zero even in an off-state, i.e. insufficient pinch-off characteristics.

SUMMARY

[0012] According to one aspect of the invention, there is provided a compound semiconductor device including:

[0013] a conductive semiconductor substrate;

[0014] a drain electrode formed on a bottom surface of the conductive semiconductor substrate;

[0015] a current blocking layer formed on a top surface of the conductive semiconductor substrate, made of high resistance compound semiconductor or insulator, and having openings;

[0016] an active layer of compound semiconductor burying the openings and extending on an upper surface of the current blocking layer;